

PATENT ABSTRACTS OF JAPAN

(11)Publication number :

09-232574

(43)Date of publication of application : 05.09.1997

(51)Int.Cl.

H01L 29/78

H01L 21/28

(21)Application number : 08-061841

(71)Applicant : SONY CORP

(22)Date of filing : 23.02.1996

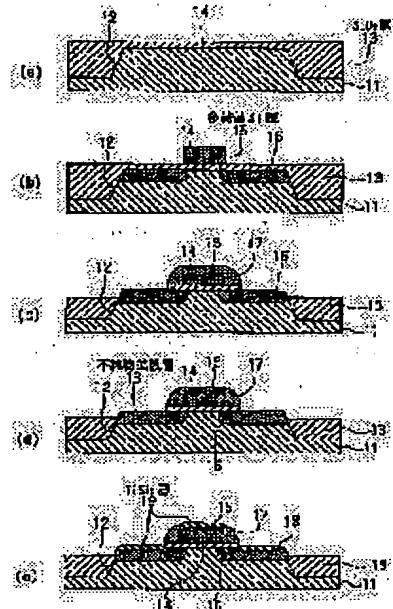
(72)Inventor : OKAMOTO YUTAKA

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the sheet resistance of an impurity diffusion layer by widening the width of the compound layer formed on the surface of the impurity diffusion layer even when the width of an element active region is the same.

SOLUTION: After the surface of the SiO₂ film 13 in an element isolation region gas been made lower than the upper surface of an Si substrate 11, a TiSi layer 19 is formed on the surface of an impurity diffusion layer 18 and a polycrystalline Si film 15. As a result, the surface of the TiSi₂ layer 19 becomes lower toward the direction of the surface of the SiO₂ film 13 on the boundary part with the SiO₂ film, and the width of the TiSi₂ layer 19 is wide even when the width of the element active region is the same. Accordingly, the sheet resistance of the impurity diffusion layer 18 is low, and current drive power and the like is high.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by the front face of the compound layer which is formed on the surface of the impurity diffused layer, and consists of the semi-conductor and the metal being low toward the front face of the insulator layer in said component isolation region in the boundary section of said impurity diffused layer and component isolation region.

[Claim 2] The manufacture approach of the semiconductor device characterized by providing the process which forms a component isolation region by the insulator layer with a front face lower than the top face of an impurity diffused layer, and the process which forms the compound layer of a semi-conductor and a metal in the front face of said impurity diffused layer.

[Claim 3] The manufacture approach of the semiconductor device according to claim 2 characterized by making the front face of said insulator layer lower than the top face of a component active region by etching said insulator layer into a gate electrode at the etchback and coincidence for forming an insulating side-attachment-wall spacer.

[Claim 4] The manufacture approach of the semiconductor device according to claim 2 characterized by forming said impurity diffused layer by the slanting revolution ion implantation of an impurity after forming said insulator layer with said front face lower than the top face of said component active region.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device with which the compound layer of a semi-conductor and a metal is formed on the surface of the impurity diffused layer, and its manufacture approach.

[0002]

[Description of the Prior Art] In order to make semiconductor devices, such as an MOS transistor, detailed, it is necessary to make an impurity diffused layer shallow for relief of a short channel effect etc. but, and if an impurity diffused layer is made shallow, sheet resistance will become high and engine performance, such as current actuation capacity, will fall. For this reason, the compound layer of a semi-conductor and a metal is formed on the surface of an impurity diffused layer, and the structure which makes sheet resistance of an impurity diffused layer low is considered.

[0003] Drawing 2 shows the 1 conventional example of the MOS transistor which has such a compound layer, and its manufacture approach. In order to manufacture this 1 conventional example, as it is shown in drawing 2 (a), the Si substrate 11 of p mold is selectively etched to a depth of 0.5 micrometers, and a trench 12 is formed, and it is SiO₂ to this trench 12. A component isolation region is formed by embedding the film 13. And SiO₂ SiO₂ whose thickness is 16nm on the front face of the component active region surrounded by the film 13. The film 14 is formed as gate oxide.

[0004] Next, as shown in drawing 2 (b), thickness makes the polycrystal Si film 15 which is 200nm deposit with a CVD method, and processes this polycrystal Si film 15 into the configuration of a gate electrode. And the resist (not shown) which has opening is formed on the formation field of the MOS transistor made into LDD structure, and they are this resist, the polycrystal Si film 15, and SiO₂. The film 13 is used as a mask and it is Phost+. An ion implantation is carried out with the acceleration energy of 30keV(s), and the dose of 3x10¹³cm⁻², and an impurity diffused layer 16 is formed.

[0005] Next, Si₃N₄ whose thickness is 150nm as shown in drawing 2 (c) The film 17 is made to deposit with a CVD method, and it is this Si₃N₄. By carrying out dry etching of the whole surface of the film 17 in different direction, it is Si₃N₄. The side-attachment-wall spacer which consists of the film 17 is formed in the polycrystal Si film 15.

[0006] Next, as shown in drawing 2 (d), the resist (not shown) which has opening is formed on the formation field of an MOS transistor, and they are this resist, the polycrystal Si film 15, and Si₃N₄. The film 17 and SiO₂ The film 13 is used as a mask and it is As+. An ion implantation is carried out with the acceleration energy of 50keV(s), and the dose of 3x10¹⁵cm⁻². And N₂ The polycrystal Si film 15 is used as n mold at the same time it performs 900 degrees C in an ambient atmosphere, and heat treatment for 20 minutes and forms the impurity diffused layer 18 as the source / a drain field.

[0007] Next, make Ti layer (not shown) whose thickness is 30nm deposit in a spatter, perform 650 degrees C and heat treatment for 30 seconds, the Si substrate 11 and the polycrystal Si film 15 which touch mutually, and Ti layer are made to react, and it is TiSi₂. A layer (not shown) is formed. And SiO₂ The film 13 and Si₃N₄ Ti layer which remains without having deposited on the film 17 and reacting with the Si substrate 11 or the polycrystal Si film 15 is removed.

[0008] Then, TiSi2 which performs 800 degrees C and heat treatment for 30 seconds, and is formed in self align on the Si substrate 11 and the polycrystal Si film 15 TiSi2 of the low resistance by the layer It is made a layer 19. This TiSi2 For a layer 19, the sheet resistance of an impurity diffused layer 18 or the polycrystal Si film 15 becomes low at several ohms / **.

[0009]

[Problem(s) to be Solved by the Invention] However, Ti layer is used especially and it is TiSi2. When a layer 19 is formed, since the component active region is narrow, the width of face of an impurity diffused layer 18 is narrow, and it is TiSi2. If the width of face of a layer 19 is also narrow, the thin line effectiveness shown in drawing 3 will arise. For this reason, the sheet resistance of an impurity diffused layer 18 does not become low enough, but it is TiSi2. The effectiveness in which the layer 19 was formed cannot fully be acquired.

[0010]

[Means for Solving the Problem] The semiconductor device of claim 1 is characterized by the front face of the compound layer which is formed on the surface of the impurity diffused layer, and consists of the semi-conductor and the metal being low toward the front face of the insulator layer in said component isolation region in the boundary section of said impurity diffused layer and component isolation region.

[0011] The manufacture approach of the semiconductor device of claim 2 is characterized by providing the process which forms a component isolation region by the insulator layer with a front face lower than the top face of an impurity diffused layer, and the process which forms the compound layer of a semi-conductor and a metal in the front face of said impurity diffused layer.

[0012] The manufacture approach of the semiconductor device of claim 3 is characterized by making the front face of said insulator layer lower than the top face of a component active region in the manufacture approach of the semiconductor device of claim 2 by etching said insulator layer into the etchback and coincidence for forming an insulating side-attachment-wall spacer in a gate electrode.

[0013] In the manufacture approach of the semiconductor device of claim 2, the manufacture approach of the semiconductor device of claim 4 is characterized by forming said impurity diffused layer by the slanting revolution ion implantation of an impurity, after said front face forms said insulator layer lower than the top face of said component active region.

[0014] since the front face of the compound layer currently formed on the surface of the impurity diffused layer is low toward the front face of the insulator layer in a component isolation region in the semiconductor device of claim 1 in the boundary section with a component isolation region, even when the width of face of a component active region is the same, compared with structure without this level difference, the width of face of a compound layer is wide.

[0015] By the manufacture approach of the semiconductor device of claim 2, since a front face forms a component isolation region by the insulator layer lower than the top face of an impurity diffused layer and forms the compound layer on the surface of an impurity diffused layer, the front face of a compound layer becomes low toward the front face of the insulator layer in a component isolation region in the boundary section with a component isolation region.

[0016] By the manufacture approach of the semiconductor device of claim 3, since it is performing making the front face of the insulator layer in a component isolation region lower than the top face of a component active region to forming an insulating side-attachment-wall spacer in a gate electrode, and coincidence, even if it makes the front face of the insulator layer in a component isolation region lower than the top face of a component active region, a production process does not increase.

[0017] By the manufacture approach of the semiconductor device of claim 4, since the impurity diffused layer is formed by the slanting revolution ion implantation of an impurity, even if it enlarges the level difference of the top face of a component active region, and the front face of the insulator layer in a component isolation region, an impurity diffused layer can be formed also in the component active region of the boundary section with a component isolation region.

[0018]

[Embodiment of the Invention] It is TiSi2 to the front face of the following, the source / drain field, and

a gate electrode. One operation gestalt of the MOS transistor of the LDD structure where the layer is formed in self align, and its manufacture approach is explained referring to drawing 1 .

[0019] Even if it faces manufacture of the MOS transistor by this operation gestalt, as it is shown in drawing 1 (c), it is Si3 N4. After forming in the polycrystal Si film 15 the side-attachment-wall spacer which consists of the film 17, it is SiO2 successingly. The film 13 is etched. This SiO2 Except for making only 0.05–0.1 micrometers of front faces of the film 13 lower than the top face of the Si substrate 11, the same process is substantially performed with the 1 conventional example shown in drawing 2 .

[0020] even when the width of face of a component active region is the same as the 1 conventional example with such an operation gestalt — the top face of the Si substrate 11, and SiO2 the part to which a level difference exists between the front faces of the film 13 — the front face of an impurity diffused layer 18 — being large — TiSi2 The width of face of a layer 19 is also wide. For this reason, it is hard to be influenced of the thin line effectiveness, and since the sheet resistance of an impurity diffused layer 18 is low, engine performance, such as current actuation capacity, is high.

[0021] In addition, at the above operation gestalt, it is Si3 N4. After forming in the polycrystal Si film 15 the side-attachment-wall spacer which consists of the film 17, it is SiO2 successingly. The film 13 is etched and it is this SiO2. Although the front face of the film 13 is made lower than the top face of the Si substrate 11, it is SiO2, for example. If a side-attachment-wall spacer is formed by the film, it is not necessary to make a change of etching gas etc., and a production process will decrease substantially.

[0022] Moreover, with the above operation gestalt, the junction depth of impurity diffused layers 16 and 18 is mutually made equal so that clearly also from drawing 1 (c) – (e), and it is SiO2. The front face of the film 13 is made shallower than this junction depth. However, it will be SiO2 if an impurity diffused layer 18 is formed by the slanting revolution ion implantation of an impurity. It is SiO2 even if it makes the front face of the film 13 deeper than the junction depth of an impurity diffused layer 16. An impurity diffused layer 18 can be formed also in the boundary section with the film 13.

[0023] For this reason, SiO2 It is TiSi2 even if it makes the front face of the film 13 deeper than the junction depth of an impurity diffused layer 16. It can prevent that a layer 19 contacts the Si substrate 11 directly, and leakage current flows through this contact section. Therefore, the front face of an impurity diffused layer 18 is further made large, and it is TiSi2. The width of face of a layer 19 can also be expanded further, can make still lower sheet resistance of an impurity diffused layer 18, and can raise engine performance, such as current actuation capacity, further.

[0024] Moreover, at the above operation gestalt, it is TiSi2 as a silicide layer to the front face of an impurity diffused layer 18 and the polycrystal Si film 15. Although the layer 19 is formed, they are silicide layers, such as Co, nickel, and Pt, TiSi2 You may form instead of a layer 19 and a silicide layer may be formed only in the front face of an impurity diffused layer 18.

[0025] Moreover, although the above operation gestalt applies this invention to the MOS transistor of LDD structure, and its manufacture, this invention is applicable also to a semiconductor device other than the MOS transistor and MOS transistor of non-LDD structure, and its manufacture.

[0026]

[Effect of the Invention] In the semiconductor device of claim 1, since the width of face of the compound layer with the same width of face of a component active region currently formed on the surface of the impurity diffused layer but is wide, the sheet resistance of an impurity diffused layer is low, and the engine performance is high.

[0027] by the manufacture approach of the semiconductor device of claim 2, since the front face of the compound layer formed on the surface of an impurity diffused layer becomes low toward the front face of the insulator layer in a component isolation region in the boundary section with a component isolation region, even when the width of face of a component active region is the same, the width of face of a compound layer is wide, and a semiconductor device with the low sheet resistance of an impurity diffused layer and the high engine performance can be manufactured.

[0028] by the manufacture approach of the semiconductor device of claim 3, since a production process does not increase even if it makes the front face of the insulator layer in a component isolation region

lower than the top face of a component active region, even when the width of face of a component active region is the same, the width of face of a compound layer is wide, and a semiconductor device with the low sheet resistance of an impurity diffused layer and the high engine performance can be manufactured by low cost.

[0029] since an impurity diffused layer can be formed also in the component active region of the boundary section with a component isolation region by the manufacture approach of the semiconductor device of claim 4 even if it enlarges the level difference of the top face of a component active region, and the front face of the insulator layer in a component isolation region, even when the width of face of a component active region is the same — a compound layer — width of face is still wider and a semiconductor device with the still lower sheet resistance of an impurity diffused layer and the still higher engine performance can be manufactured.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original
precisely.

2.**** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional side elevation showing the manufacture approach of 1 operation gestalt of
this invention in order of a process.

[Drawing 2] It is the sectional side elevation showing the manufacture approach of the 1 conventional
example of this invention in order of a process.

[Drawing 3] It is a graph for explaining the thin line effectiveness.

[Description of Notations]

13 SiO₂ Film 15 Polycrystal Si Film

18 Impurity Diffused Layer 19 TiSi₂ Layer

[Translation done.]

(19)日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平9-232574

(43)公開日 平成9年(1997)9月5日

(51)Int.Cl.⁶

H 0 1 L 29/78
21/28

識別記号

3 0 1

庁内整理番号

F I

H 0 1 L 29/78
21/28
29/78

技術表示箇所

3 0 1 R
3 0 1 T
3 0 1 X

審査請求 未請求 請求項の数4 FD (全5頁)

(21)出願番号 特願平8-61841

(22)出願日 平成8年(1996)2月23日

(71)出願人 000002185

ソニー株式会社

東京都品川区北品川6丁目7番35号

(72)発明者 岡本 裕

東京都品川区北品川6丁目7番35号 ソニー株式会社内

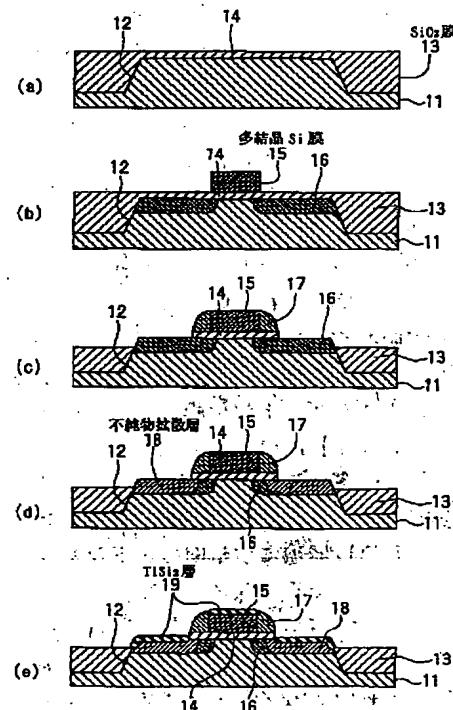
(74)代理人 弁理士 土屋 勝

(54)【発明の名称】 半導体装置及びその製造方法

(57)【要約】

【課題】 素子活性領域の幅が同じでも、不純物拡散層の表面に形成されている化合物層の幅を広くして不純物拡散層のシート抵抗を低くする。

【解決手段】 素子分離領域におけるSiO₂膜13の表面をSi基板11の上面よりも低くした後、不純物拡散層18及び多結晶Si膜15の表面にTiSi₂層19を形成する。このため、TiSi₂層19の表面がSiO₂膜13との境界部においてSiO₂膜13の表面に向かって低くなり、この段差がない構造に比べて、素子活性領域の幅が同じでもTiSi₂層19の幅が広い。従って、不純物拡散層18のシート抵抗が低く、電流駆動能力等が高い。



(2)

2

【特許請求の範囲】

【請求項1】 不純物拡散層の表面に形成されており半導体と金属とから成っている化合物層の表面が、前記不純物拡散層と素子分離領域との境界部において前記素子分離領域における絶縁膜の表面に向かって低くなっていることを特徴とする半導体装置。

【請求項2】 表面が不純物拡散層の上面よりも低い絶縁膜で素子分離領域を形成する工程と、

半導体と金属との化合物層を前記不純物拡散層の表面に形成する工程とを具備することを特徴とする半導体装置の製造方法。

【請求項3】 ゲート電極に絶縁性の側壁スペーサを形成するためのエッチパックと同時に前記絶縁膜をエッチングすることによって、前記絶縁膜の表面を素子活性領域の上面よりも低くすることを特徴とする請求項2記載の半導体装置の製造方法。

【請求項4】 前記表面が前記素子活性領域の上面よりも低い前記絶縁膜を形成した後に、不純物の斜め回転イオン注入によって前記不純物拡散層を形成することを特徴とする請求項2記載の半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本願の発明は、半導体と金属との化合物層が不純物拡散層の表面に形成されている半導体装置及びその製造方法に関するものである。

【0002】

【従来の技術】 MOSトランジスタ等の半導体装置を微細化するためには、短チャネル効果の軽減等のために不純物拡散層を浅くする必要があるが、不純物拡散層を浅くすると、シート抵抗が高くなっている電流駆動能力等の性能が低下する。このため、半導体と金属との化合物層を不純物拡散層の表面に形成して、不純物拡散層のシート抵抗を低くする構造が考えられている。

【0003】 図2は、この様な化合物層を有するMOSトランジスタ及びその製造方法の一従来例を示している。この一従来例を製造するためには、図2(a)に示す様に、p型のSi基板11を0.5μmの深さまで選択的にエッチングしてトレンチ12を形成し、このトレンチ12にSiO₂膜13を埋め込むことによって素子分離領域を形成する。そして、SiO₂膜13に囲まれている素子活性領域の表面に、膜厚が16nmのSiO₂膜14をゲート酸化膜として形成する。

【0004】 次に、図2(b)に示す様に、膜厚が200nmの多結晶Si膜15をCVD法で堆積させ、この多結晶Si膜15をゲート電極の形状に加工する。そして、LDD構造にするMOSトランジスタの形成領域上に開口を有するレジスト(図示せず)を形成し、このレジスト、多結晶Si膜15及びSiO₂膜13をマスクにして、Phos⁺を30keVの加速エネルギー及び3×10¹³cm⁻²のドーズ量でイオン注入して不純物拡

散層16を形成する。

【0005】 次に、図2(c)に示す様に、膜厚が150nmのSi₃N₄膜17をCVD法で堆積させ、このSi₃N₄膜17の全面を異方的にドライエッチングすることによって、Si₃N₄膜17から成る側壁スペーサを多結晶Si膜15に形成する。

【0006】 次に、図2(d)に示す様に、MOSトランジスタの形成領域上に開口を有するレジスト(図示せず)を形成し、このレジスト、多結晶Si膜15、Si₃N₄膜17及びSiO₂膜13をマスクにして、As⁺を50keVの加速エネルギー及び3×10¹⁵cm⁻²のドーズ量でイオン注入する。そして、N₂雰囲気中における900°C、20分間の熱処理を行って、ソース/ドレイン領域としての不純物拡散層18を形成すると同時に、多結晶Si膜15をn型にする。

【0007】 次に、膜厚が30nmのTi層(図示せず)をスパッタ法で堆積させ、650°C、30秒間の熱処理を行って、互いに接触しているSi基板11及び多結晶Si膜15とTi層とを反応させてTi₂Si₂層

(図示せず)を形成する。そして、SiO₂膜13及びSi₃N₄膜17上に堆積していくSi基板11または多結晶Si膜15と反応せずに残っているTi層を除去する。

【0008】 その後、800°C、30秒間の熱処理を行って、Si基板11上及び多結晶Si膜15上に自己整合的に形成されているTi₂Si₂層を低抵抗のTi₂Si₂層19にする。このTi₂Si₂層19のために、不純物拡散層18や多結晶Si膜15のシート抵抗は数Ω/□に低くなる。

【0009】

【発明が解決しようとする課題】 しかし、特に、Ti層を用いてTi₂Si₂層19を形成した場合、素子活性領域が狭いために不純物拡散層18の幅が狭くてTi₂Si₂層19の幅も狭いと、図3に示す細線効果が生じる。このため、不純物拡散層18のシート抵抗が十分には低くならず、Ti₂Si₂層19を形成した効果を十分には得ることができない。

【0010】

【課題を解決するための手段】 請求項1の半導体装置は、不純物拡散層の表面に形成されており半導体と金属とから成っている化合物層の表面が、前記不純物拡散層と素子分離領域との境界部において前記素子分離領域における絶縁膜の表面に向かって低くなっていることを特徴としている。

【0011】 請求項2の半導体装置の製造方法は、表面が不純物拡散層の上面よりも低い絶縁膜で素子分離領域を形成する工程と、半導体と金属との化合物層を前記不純物拡散層の表面に形成する工程とを具備することを特徴としている。

【0012】 請求項3の半導体装置の製造方法は、請求

(3)

3

項2の半導体装置の製造方法において、ゲート電極に絶縁性の側壁スペーサを形成するためのエッチバックとともに前記絶縁膜をエッチングすることによって、前記絶縁膜の表面を素子活性領域の上面よりも低くすることを特徴としている。

【0013】請求項4の半導体装置の製造方法は、請求項2の半導体装置の製造方法において、前記表面が前記素子活性領域の上面よりも低い前記絶縁膜を形成した後に、不純物の斜め回転イオン注入によって前記不純物拡散層を形成することを特徴としている。

【0014】請求項1の半導体装置では、不純物拡散層の表面に形成されている化合物層の表面が素子分離領域との境界部において素子分離領域における絶縁膜の表面に向かって低くなっているので、この段差がない構造に比べて、素子活性領域の幅が同じでも化合物層の幅が広い。

【0015】請求項2の半導体装置の製造方法では、表面が不純物拡散層の上面よりも低い絶縁膜で素子分離領域を形成し、不純物拡散層の表面に化合物層を形成しているので、化合物層の表面が素子分離領域との境界部において素子分離領域における絶縁膜の表面に向かって低くなる。

【0016】請求項3の半導体装置の製造方法では、素子分離領域における絶縁膜の表面を素子活性領域の上面よりも低くすることを、ゲート電極に絶縁性の側壁スペーサを形成することと同時にやっているので、素子分離領域における絶縁膜の表面を素子活性領域の上面より低くしても製造工程は増加しない。

【0017】請求項4の半導体装置の製造方法では、不純物の斜め回転イオン注入によって不純物拡散層を形成しているので、素子活性領域の上面と素子分離領域における絶縁膜の表面との段差を大きくしても、素子分離領域との境界部の素子活性領域にも不純物拡散層を形成することができる。

【0018】

【発明の実施の形態】以下、ソース／ドレイン領域及びゲート電極の表面にTiSi₂層が自己整合的に形成されているLDD構造のMOSトランジスタ及びその製造方法の一実施形態を、図1を参照しながら説明する。

【0019】本実施形態によるMOSトランジスタの製造に際しても、図1(c)に示す様に、Si₃N₄膜17から成る側壁スペーサを多結晶Si膜15に形成した後、引き続きSiO₂膜13をエッチングして、このSiO₂膜13の表面をSi基板11の上面よりも0.05～0.1μmだけ低くすることを除いて、図2に示した一従来例と実質的に同様の工程を実行する。

【0020】この様な実施形態では、素子活性領域の幅が一従来例と同じでも、Si基板11の上面とSiO₂膜13の表面との間に段差が存在する分だけ、不純物拡散層18の表面が広くてTiSi₂層19の幅も広い。

(4)

4

このため、細線効果の影響を受けにくく、不純物拡散層18のシート抵抗が低いので、電流駆動能力等の性能が高い。

【0021】なお、以上の実施形態では、Si₃N₄膜17から成る側壁スペーサを多結晶Si膜15に形成した後、引き続きSiO₂膜13をエッチングして、このSiO₂膜13の表面をSi基板11の上面よりも低くしているが、例えば、SiO₂膜で側壁スペーサを形成すれば、エッチングガスの変更等を行う必要がなく、製造工程が実質的に少なくなる。

【0022】また、以上の実施形態では、図1(c)～(e)からも明らかな様に、不純物拡散層16、18の接合深さを互いに等しくして、SiO₂膜13の表面をこの接合深さよりも浅くしている。しかし、不純物の斜め回転イオン注入によって不純物拡散層18を形成すれば、SiO₂膜13の表面を不純物拡散層16の接合深さよりも深くしても、SiO₂膜13との境界部にも不純物拡散層18を形成することができる。

【0023】このため、SiO₂膜13の表面を不純物拡散層16の接合深さよりも深くしても、TiSi₂層19がSi基板11と直接に接触しこの接触部を介してリード電流が流れることを防止することができる。従って、不純物拡散層18の表面を更に広くしてTiSi₂層19の幅も更に広げることができ、不純物拡散層18のシート抵抗を更に低くして、電流駆動能力等の性能を更に高めることができる。

【0024】また、以上の実施形態では、不純物拡散層18及び多結晶Si膜15の表面にシリサイド層としてTiSi₂層19を形成しているが、Co、Ni、Pt等のシリサイド層をTiSi₂層19の代わりに形成してもよく、不純物拡散層18の表面にのみシリサイド層を形成してもよい。

【0025】また、以上の実施形態はLDD構造のMOSトランジスタ及びその製造に本願の発明を適用したものであるが、非LDD構造のMOSトランジスタやMOSトランジスタ以外の半導体装置及びその製造にも本願の発明を適用することができる。

【0026】

【発明の効果】請求項1の半導体装置では、素子活性領域の幅が同じでも、不純物拡散層の表面に形成されている化合物層の幅が広いので、不純物拡散層のシート抵抗が低くて、性能が高い。

【0027】請求項2の半導体装置の製造方法では、不純物拡散層の表面に形成する化合物層の表面が素子分離領域との境界部において素子分離領域における絶縁膜の表面に向かって低くなっているので、素子活性領域の幅が同じでも化合物層の幅が広く、不純物拡散層のシート抵抗が低くて、性能が高い半導体装置を製造することができる。

【0028】請求項3の半導体装置の製造方法では、素

(4)

5

子分離領域における絶縁膜の表面を素子活性領域の上面より低くしても製造工程は増加しないので、素子活性領域の幅が同じでも化合物層の幅が広く、不純物拡散層のシート抵抗が低くて、性能が高い半導体装置を低コストで製造することができる。

【0029】請求項4の半導体装置の製造方法では、素子活性領域の上面と素子分離領域における絶縁膜の表面との段差を大きくしても、素子分離領域との境界部の素子活性領域にも不純物拡散層を形成することができるので、素子活性領域の幅が同じでも化合物層の更に幅が広く、不純物拡散層のシート抵抗が更に低くて、性能が更

に高い半導体装置を製造することができる。

【図面の簡単な説明】

【図1】本願の発明の一実施形態の製造方法を工程順に示す側断面図である。

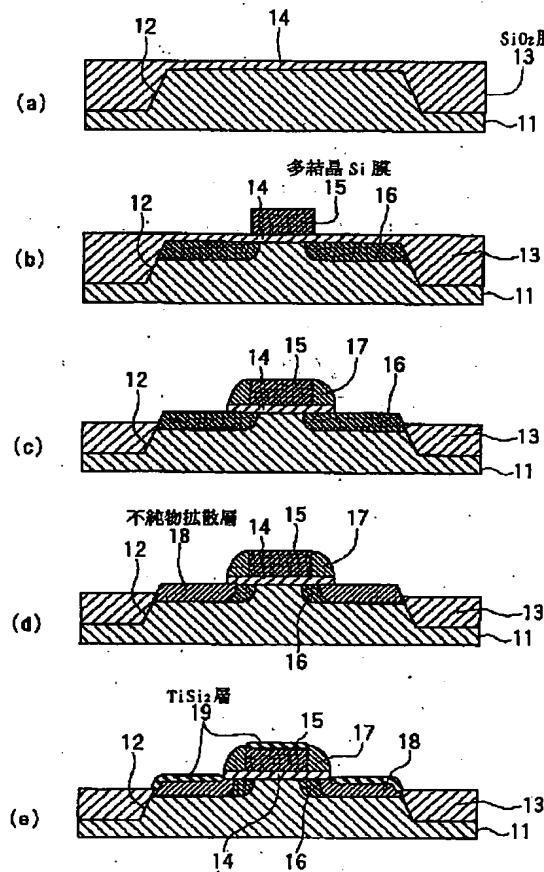
【図2】本願の発明の一従来例の製造方法を工程順に示す側断面図である。

【図3】細線効果を説明するためのグラフである。

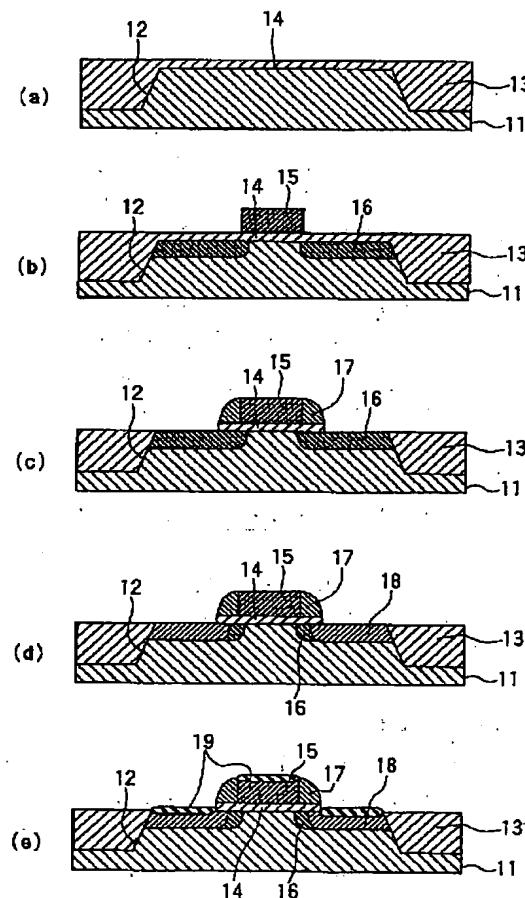
【符号の説明】

13 SiO ₂ 膜	15 多結晶Si膜
18 不純物拡散層	19 TiSi ₂ 層

【図1】

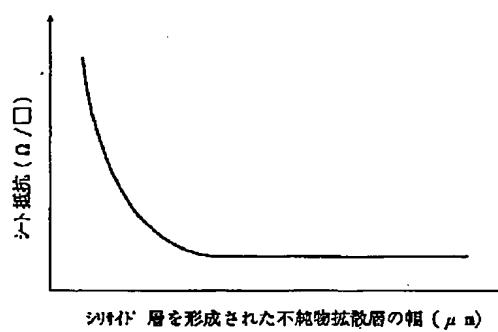


【図2】



(5)

【図3】



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.